1. (Amended) Apparatus for converting low level input signals to CMOS level output signals, said apparatus comprising:

(a) a pre-amplifier coupled to receive said low level input signals,

(b) an output buffer operatively coupled to receive an output of said pre-amplifier, said output buffer having a first transistor in an emitter follower configuration, with the load of said emitter follower provided by a second transistor, [and]

(c) a circuit for generating a drive signal, said drive signals serving to turn off said second transistor when the desired output of said emitter follower is a preselected logic level, and

(d) a second buffer circuit operatively coupling said one output of said pre-amplifier to said output buffer.

37. (Amended) Apparatus for converting low level input signals to CMOS level signals, said apparatus comprising:

(a) a pre-amplifier coupled to receive said low level input signals and for producing two output signals, said two output signals being at opposite logic levels,

(b) first and second output buffers each operatively coupled to receive a different of said two output signals, each of said first and second output buffers having an emitter follower transistor, with the load of said emitter follower transistor provided by a second transistor, [and]

(c) a circuit for providing different drive signals for each of said second transistors, each said drive signal serving to turn off one of said second transistors when the desired output of the corresponding emitter follower is a preselected logic level, and

(d) intermediate buffer circuits, the first operatively coupling a first output of said pre-amplifier to said first output buffer and the second operatively coupling a second output of said pre-amplifier to a second output buffer.

57. (Amended) A method for converting low level input signals to CMOS level output signals, said method comprising the steps of:

(a) applying said low level input signals to a pre-amplifier,

(b) operatively coupling a first output of said pre-amplifier to an output buffer, said output buffer having a first transistor in an emitter follower configuration, with the load of said emitter follower provided by a second transistor, [and]

(c) generating a drive signals, said drive signals serving to turn off said second transistor when the desired output of said emitter follower is a preselected logic level, and

(d) applying said first output of said pre-amplifier to an intermediate buffer circuit and applying the output of said buffer circuit to said output buffer.